

VLSI Design

Lecture 10: Layout, Simulation

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Adapted from lecture notes prepared by the author (from Prentice
Hall PTR)

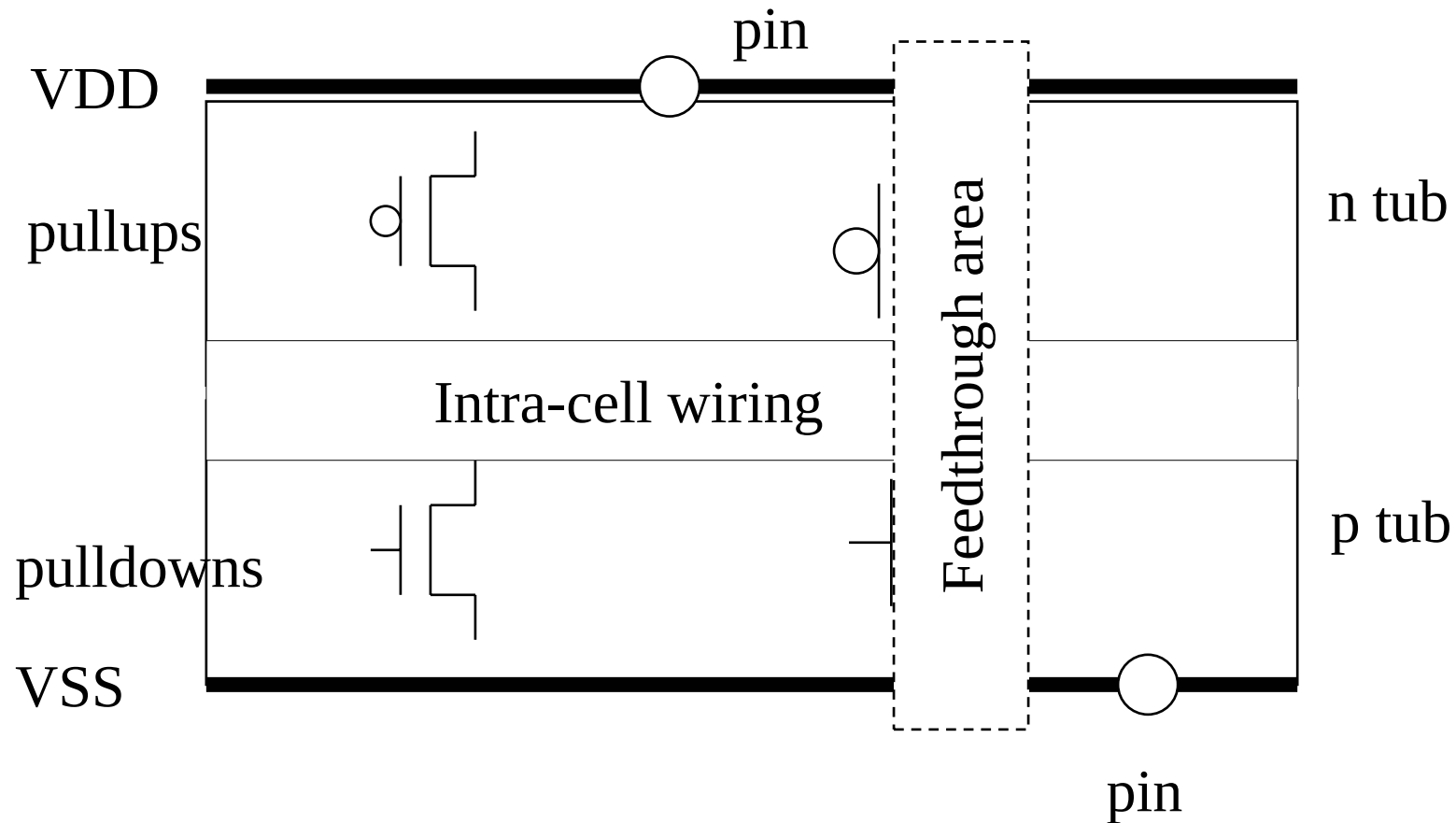
Topics

- Layouts for logic networks.
- Channel routing.
- Simulation.

Standard cell layout

- Layout made of small cells: gates, flip-flops, etc.
- Cells are hand-designed.
- Assembly of cells is automatic:
 - cells arranged in rows;
 - wires routed between (and through) cells.

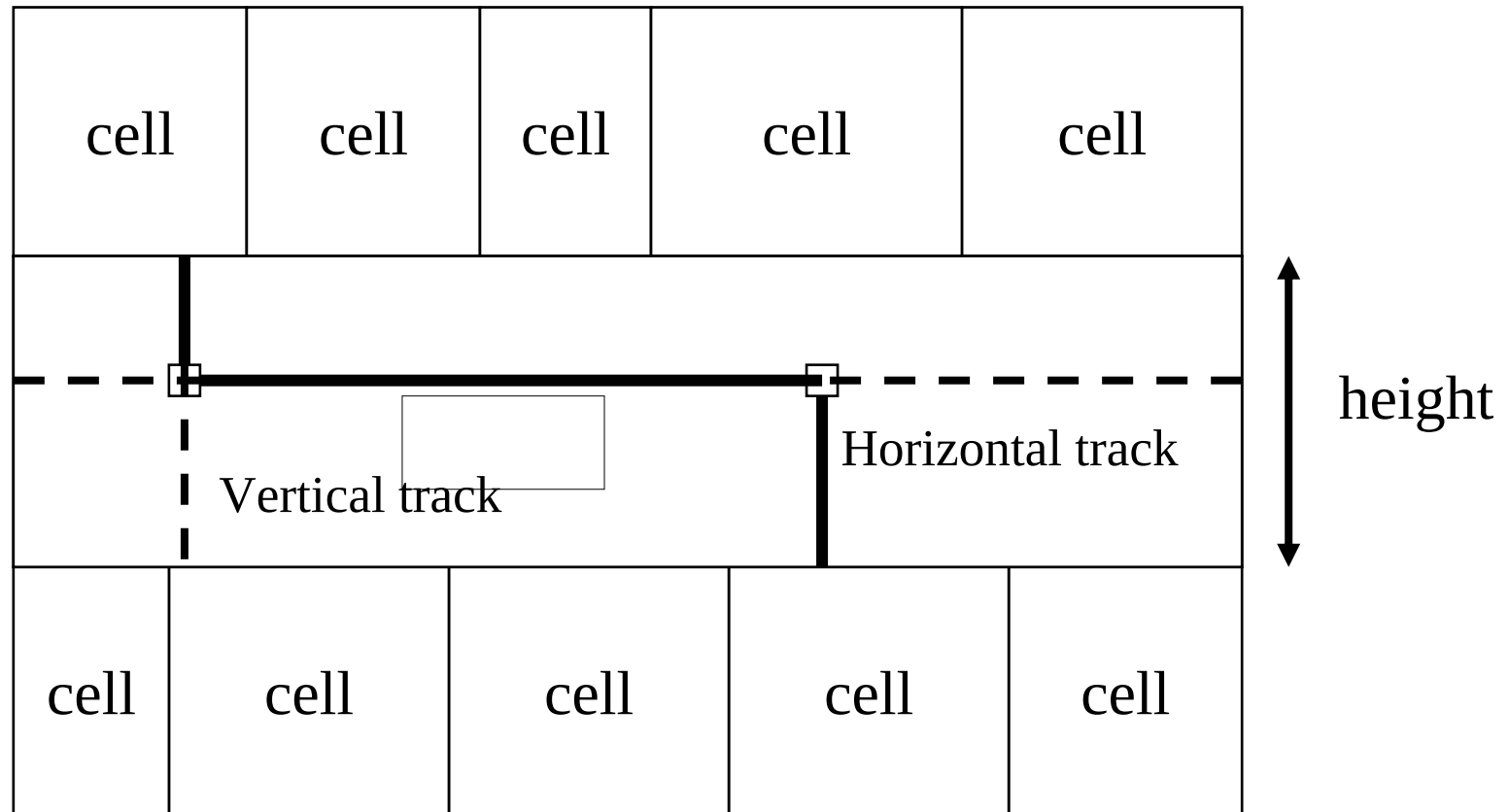
Standard cell structure



Standard cell design

- Pitch: height of cell.
 - All cells have same pitch, may have different widths.
- V_{DD} , V_{SS} connections are designed to run through cells.
- A feedthrough area may allow wires to be routed over the cell.

Single-row layout design



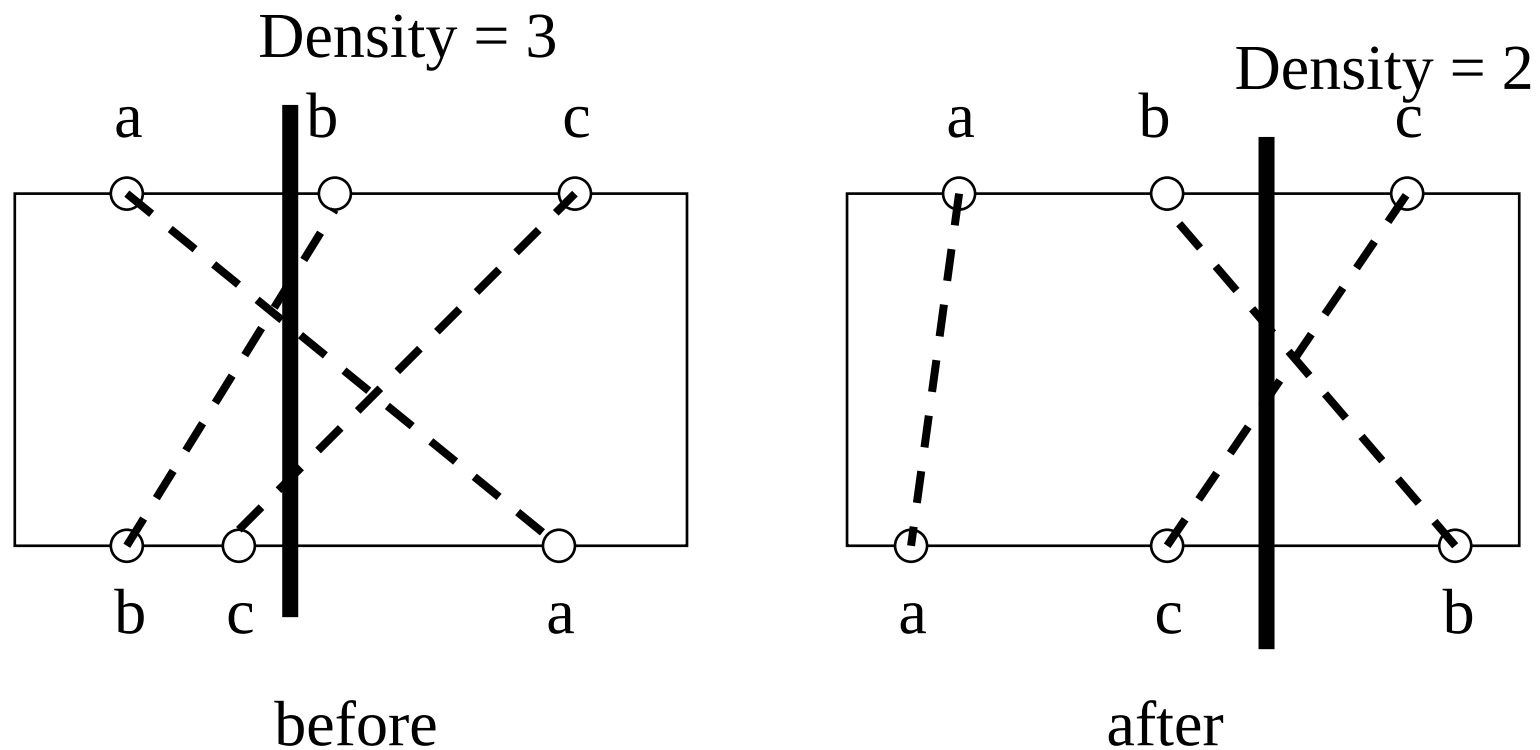
Routing channels

- Tracks form a grid for routing.
 - Spacing between tracks is center-to-center distance between wires.
 - Track spacing depends on wire layer used.
- Different layers are (generally) used for horizontal and vertical wires.
 - Horizontal and vertical can be routed relatively independently.

Routing channel design

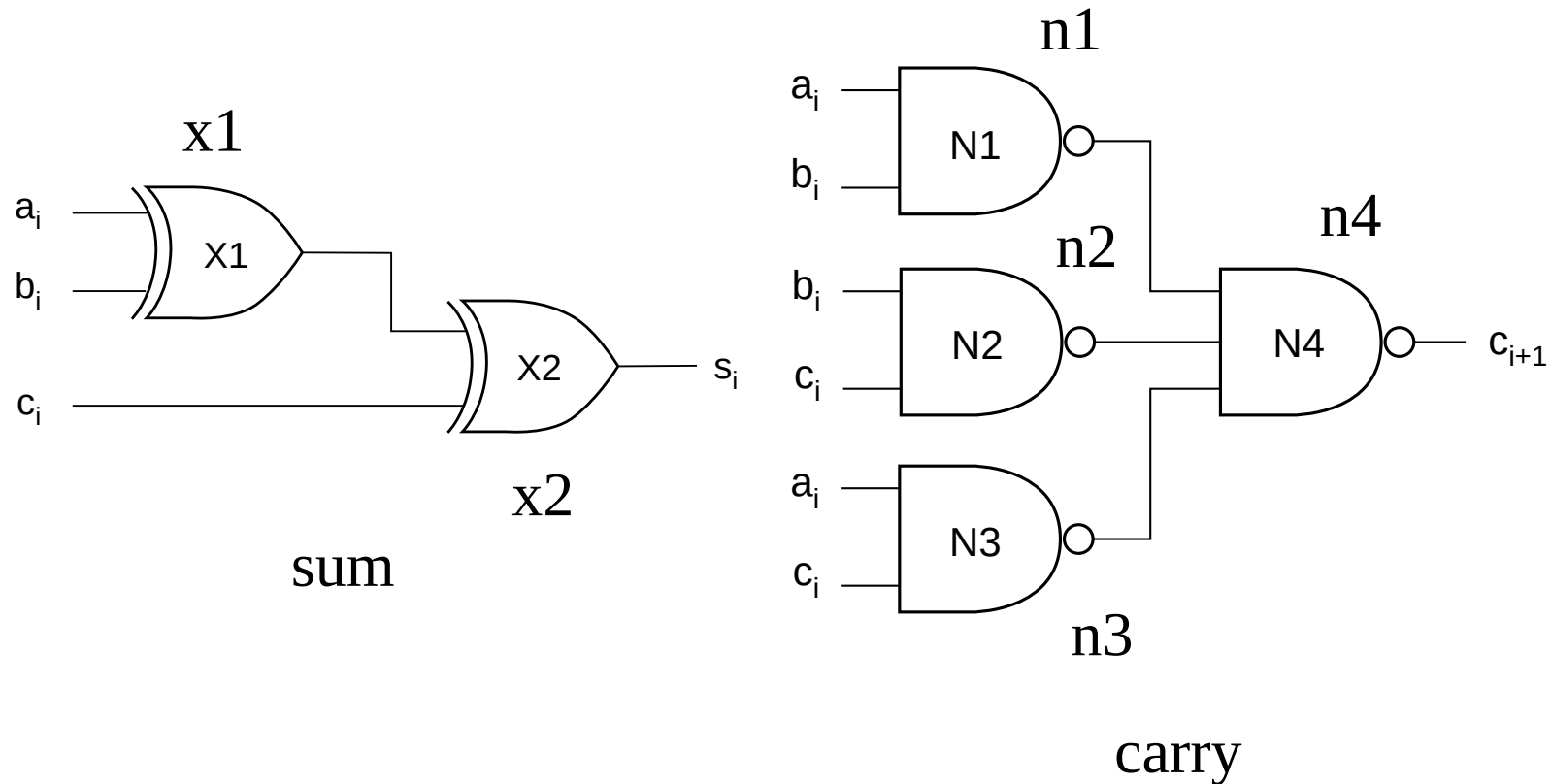
- Placement of cells determines placement of pins.
- Pin placement determines difficulty of routing problem.
- Density: lower bound on number of horizontal tracks needed to route the channel.
 - Maximum number of nets crossing from one end of channel to the other.

Pin placement and routing



Example: full adder layout

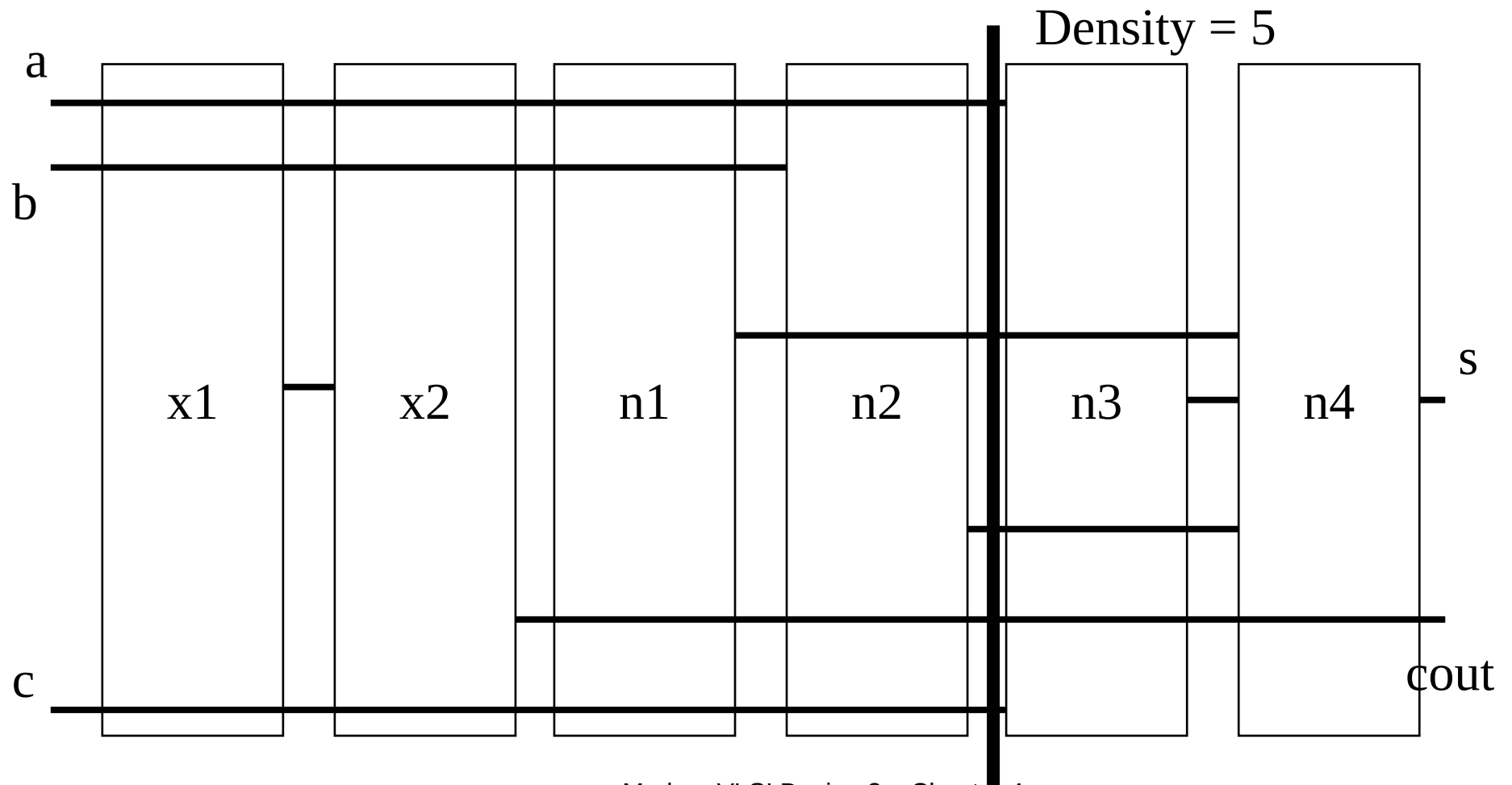
- Two outputs: sum, carry.



Layout methodology

- Generate candidates, evaluate area and speed.
 - Can improve candidate without starting from scratch.
- To generate a candidate:
 - place gates in a row;
 - draw wires between gates and primary inputs/outputs;
 - measure channel density.

A candidate layout

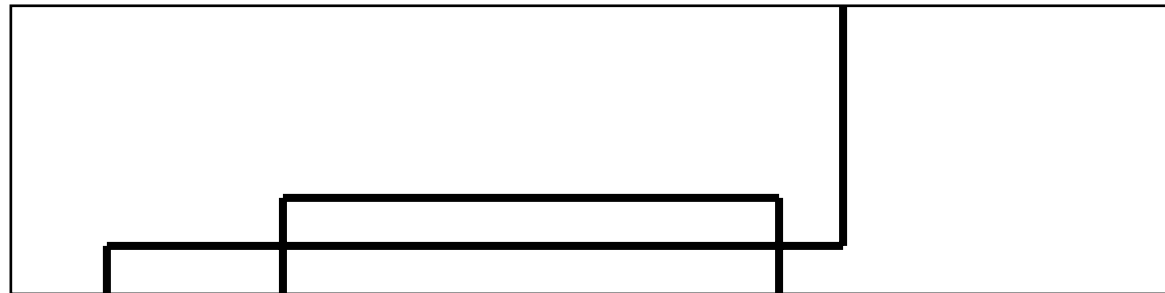


Improvement strategies

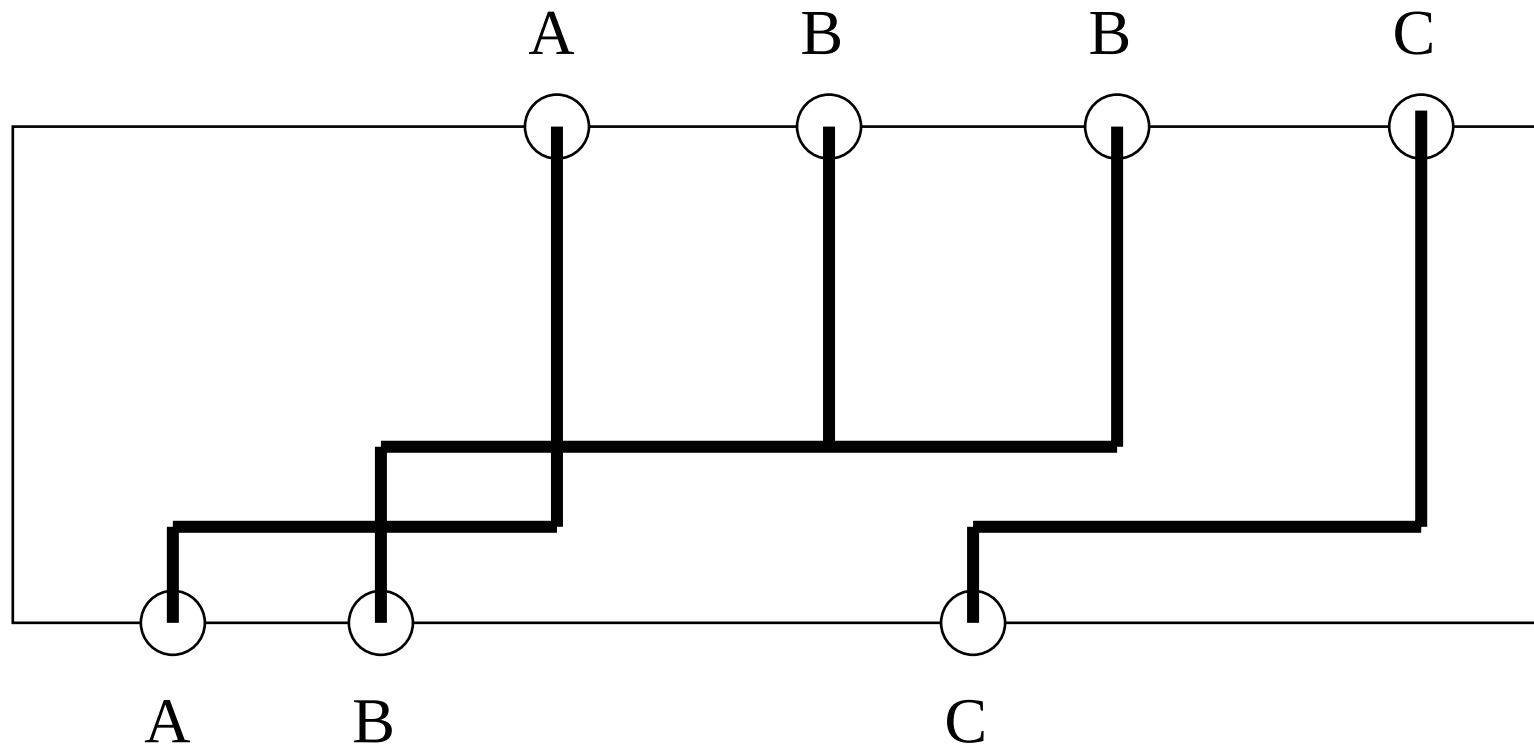
- Swap pairs of gates.
 - Doesn't help here.
- Exchange larger groups of cells.
 - Swapping order of sum and carry groups doesn't help either.
- This seems to be the placement that gives the lowest channel density.
 - Cell sizes are fixed, so channel height determines area.

Left-edge algorithm

- Basic channel routing algorithm.
- Assumes one horizontal segment per net.
- Sweep pins from left to right:
 - assign horizontal segment to lowest available track.

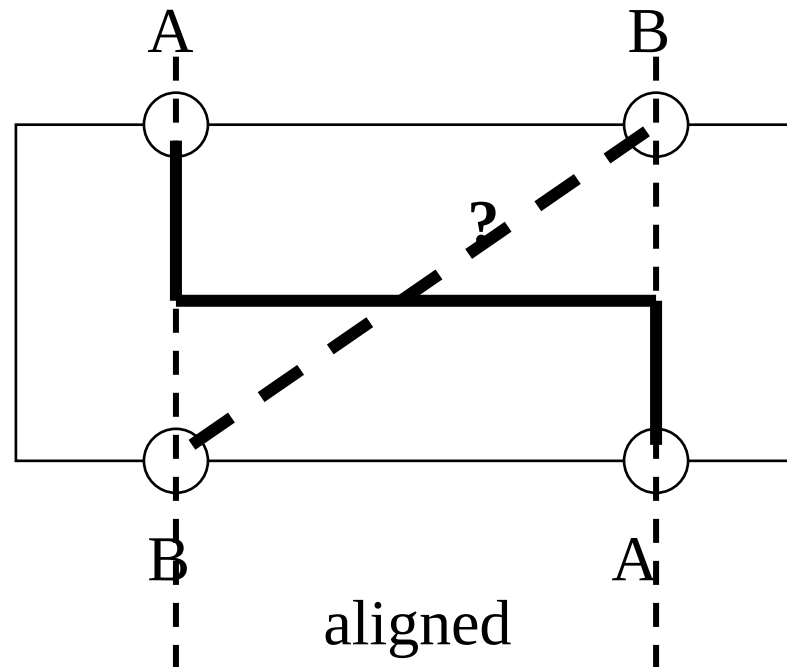


Example



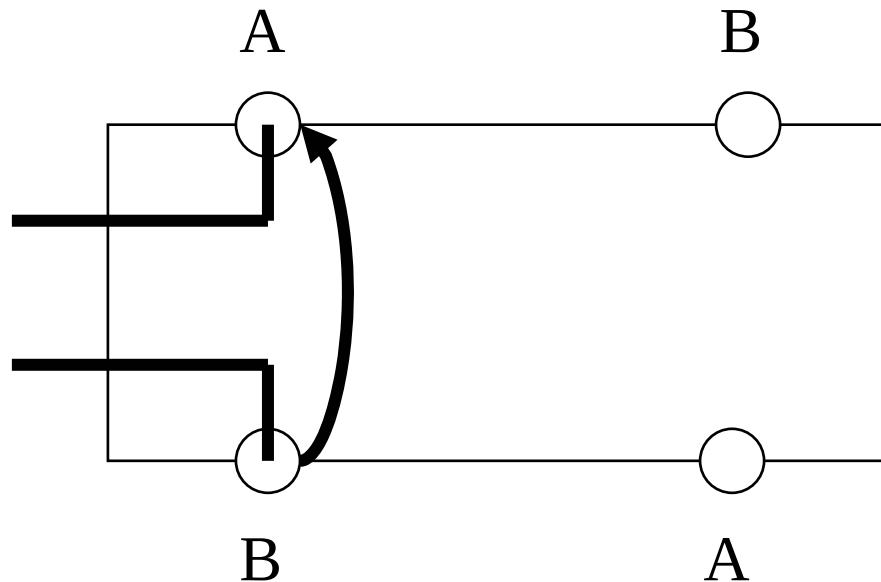
Limitations of left-edge algorithm

- Some combinations of nets require more than one horizontal segment per net.



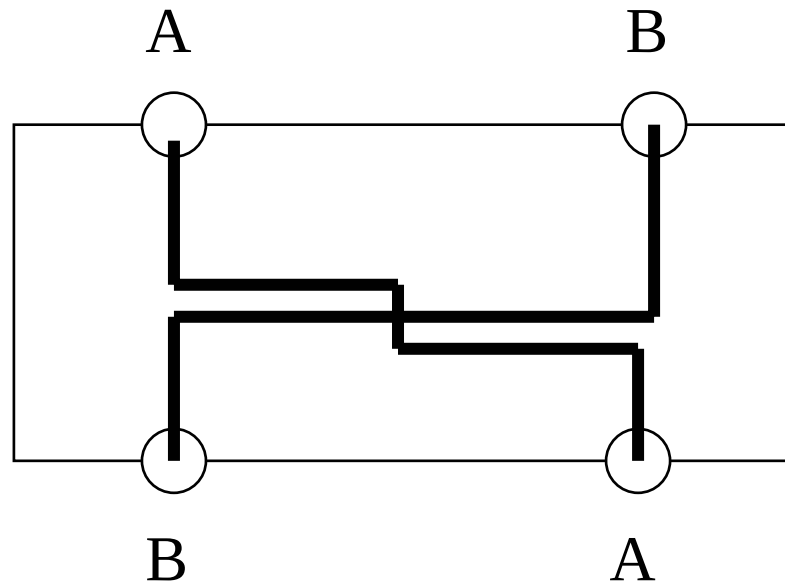
Vertical constraints

- Aligned pins form vertical constraints.
 - Wire to lower pin must be on lower track; wire to upper pin must be above lower pin's wire.



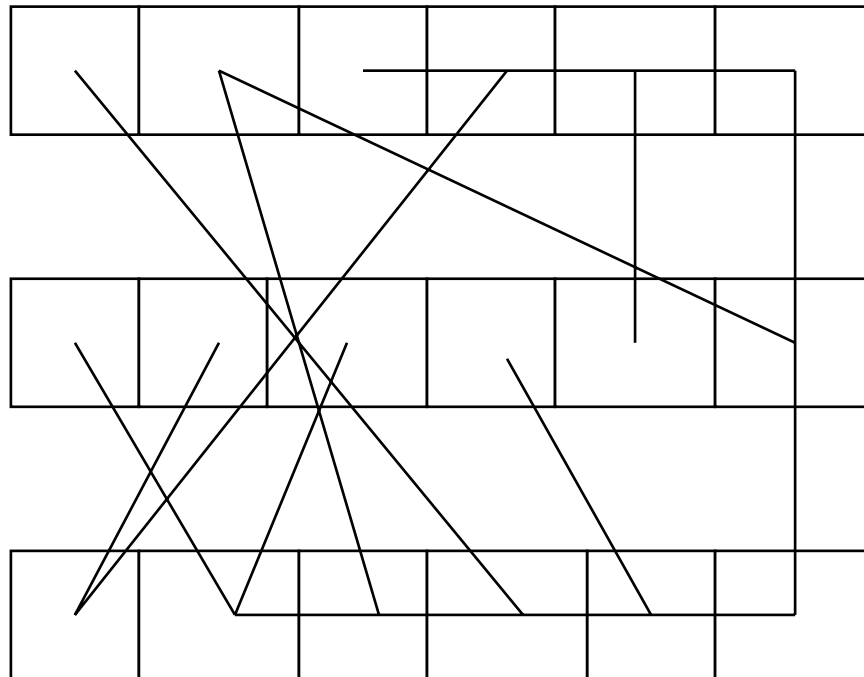
Dogleg wire

- A dogleg wire has more than one horizontal segment.



Rat's nest plot

- Can be used to judge placement before final routing.



Simulation

- Goals of simulation:
 - functional verification;
 - timing;
 - power consumption;
 - testability.

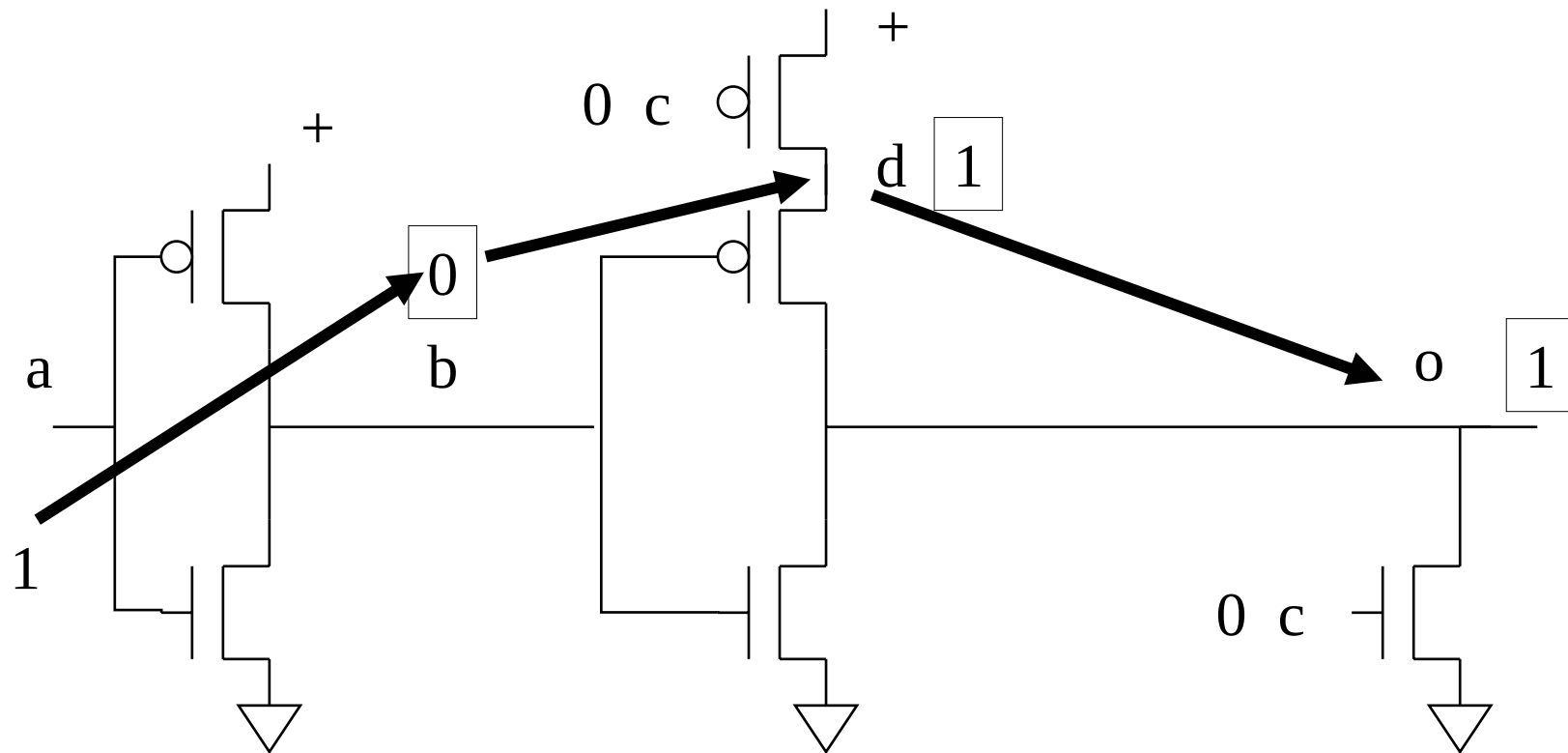
Types of simulation

- Circuit simulation:
 - analog voltages and currents.
- Timing simulation:
 - simple analog models to provide timing but not detailed waveforms.
- Switch simulation:
 - transistors as semi-ideal switches.

Types of simulation, cont'd.

- Gate simulation:
 - logic gates as primitive elements.
- Models for gate simulation:
 - zero delay;
 - unit delay;
 - variable delay.
- Fault simulation:
 - models fault propagation (more later).

Example: switch simulation



Example, cont'd.

